

**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1. (Currently amended) A method of performing latch up check on an integrated circuit (IC) design comprising the steps of:

~~computing a combined least enclosing rectangle enclosing rectangular shape that encloses~~  
a conductor region shape and contact shapes on the integrated circuit design, said rectangle shape  
being the smallest rectangular shape that completely encloses the conductor region shape and the  
contact shapes;

rasterizing the conductor region shape and the contact shapes;

iteratively expanding the contact shapes within the conductor region shape using a cellular algorithm;

generating shapes representing an unreachable area of the conductor region shape; ~~and~~

checking the shapes representing the unreachable area of the conductor region shape against junction shapes in the integrated circuit design, and reporting to a designer any junction shapes which intersect the unreachable area as errors;

representing the contact shapes as cells in a byte array;

exploring the conductor region shape by expanding the conductor region shape into  
neighboring cells of the byte array; and

periodically skipping expanding corner cells of the contact shapes.

2. (Cancel)

3. (Cancel)

4. (Currently Amended) The method, according to claim [[2]] 1, further including the step of restricting the number of directions in which the cells can expand.

5. (Previously presented) The method, according to claim 1, further including the step of creating a 2-dimensional byte array of sufficient size to rasterize the enclosing rectangle at a resolution of "I", wherein the width and height of each cell in the array corresponds to the value "I" .

6. (Previously presented) The method, according to claim 5, further including the step of initializing each cell of the byte array to a first code representing an empty cell.

7. (Previously presented) The method, according to claim 6, further including the step of converting the least enclosing rectangle to raster format in the byte array by inserting a second code into each cell intersected by an edge of the rectangle shape.

8. (Previously presented) The method, according to claim 7, further comprising the step of converting the conductor region shape to raster format in the byte array by inserting a third code into each cell intersected by an edge of the conductor region shape.

9. (Previously presented) The method, according to claim 8, further comprising the steps of:

converting the contact shapes to raster format in the byte array by inserting a fourth code into each cell intersected by an edge of a contact shape; and  
recording the address of each of these cells in a frontier list.

10. (Previously presented) The method, according to claim 9, further comprising the step of establishing a maximum distance to be searched.

11. (Previously presented) The method, according to claim 10, further comprising the steps of:

expanding the contact shapes by traversing the frontier list one cell at a time and  
examining the cell's neighbor cells as to whether they are empty or not;

inserting a fifth code into the neighbor cell and recording its location in a new frontier list if a neighbor cell is empty; and  
not expanding into it if a neighbor cell is not empty.

12. (Previously presented) The method, according to claim 11, further comprising the steps of:

expanding cells which are recorded in the new frontier list; and  
inserting a fifth code into the neighbor cell and recording its location in the new frontier list if a neighbor cell is empty; and  
not expanding into it if a neighbor cell is not empty.

13. (Previously presented) The method, according to claim 12, further comprising the steps of:

continuing to expand cells by traversing the new frontier list one cell at a time, and  
examining the cell's neighbor cells; and  
inserting a sixth code into the cell, and record its location in a third frontier list if a neighbor cell is empty.

14. (Currently Amended) A method of performing latch up check on an integrated circuit (IC) design comprising the steps of:

computing a combined least enclosing rectangle enclosing rectangular shape that encloses a conductor region shape and contact shapes on the integrated circuit design, said rectangle shape being the smallest rectangular shape that completely encloses the conductor region shape and the contact shapes;

rasterizing the conductor region shape and the contact shapes;  
iteratively expanding the contact shapes within the conductor region shape using a cellular algorithm;  
generating shapes representing an unreachable area of the conductor region shape; and  
checking the shapes representing the unreachable area of the conductor region shape against junction shapes in the design, and reporting to a designer any junction shapes which

intersect the unreachable area as errors;

creating a 2-dimensional byte array of sufficient size to rasterize the enclosing rectangle at a resolution of "I", wherein the width and height of each cell in the array corresponds to the value "I";

initializing each cell of the byte array to a first code representing an empty cell;

converting the least enclosing rectangle to raster format in the byte array by inserting a second code into each cell intersected by an edge of the rectangle shape;

converting the conductor region shape to raster format in the byte array by inserting a third code into each cell intersected by an edge of the conductor region shape;

converting the contact shapes to raster format in the byte array by inserting a fourth code into each cell intersected by an edge of a contact shape;

recording the address of each of these cells in a frontier list;

establishing a maximum distance to be searched;

expanding the contact shapes by traversing the frontier list one cell at a time and

examining the cell's neighbor cells as to whether they are empty or not;

inserting a fifth code into the neighbor cell and recording its location in a new frontier list if a neighbor cell is empty and not expanding into it if a neighbor cell is not empty;

expanding cells which are recorded in the new frontier list;

inserting a fifth code into the neighbor cell and recording its location in the new frontier list if a neighbor cell is empty and not expanding into it if a neighbor cell is not empty;

continuing to expand cells by traversing the new frontier list one cell at a time, and examining the cell's neighbor cells; and

inserting a sixth code into the cell, and record its location in a third frontier list if a neighbor cell is empty; and

further comprising the step of extracting an unreachable area of the conductor region by traversing the byte array, row-by-row, detecting horizontal chains of unreachable cells, converting each chain into a rectangle by converting its corners into (X,Y) coordinate pairs representing positions in an original drawing space, and computing the union of these rectangles, and returning these shape(s) as the unreachable area of the conductor region.

15. (Previously presented) The method, according to claim 14, further comprising the steps of:

extracting an unreachable area of the contact region by converting each unreachable cell in the byte array to a square;

unionizing all the unreachable cells; and

returning these shape(s) as the unreachable area of the conductor region.

16. (Original) A method of performing latch up check on an integrated circuit (IC) design comprising the steps of:

rasterizing vector domain images of a conductor region shape and well contact shapes;

iteratively expanding the well contact shapes using a cellular algorithm;

extracting unreachable areas of the conductor region shape by detecting chains of unreachable cells;

converting unreachable areas into shapes, and returning these shapes as unreachable areas in the vector domain;

checking the unreachable areas against junction shapes in the design; and

flagging any junction shapes which intersect the unreachable areas as errors.

17. (Original) A computer program product comprising:

a computer usable medium having computer readable program code means embodied therein for performing latch up check on an integrated circuit (IC) design;

computer readable program code means for causing a computer to rasterize vector domain images of a conductor region shape and well contact shapes;

computer readable program code means for causing the computer to iteratively expand the contact shapes using a cellular algorithm;

computer readable program code means for causing the computer to extract unreachable areas of the conductor region shape by detecting chains of unreachable cells;

computer readable program code means for causing the computer to convert unreachable areas into shapes, and returning these shapes as unreachable areas in the vector domain; and

computer readable program code means for causing the computer to check the

unreachable areas in the vector domain against junction shapes in the design, and to flag any junction shapes which intersect the unreachable areas as errors.

18. (Previously presented) The computer program product, according to claim 17, further comprising:

computer readable program code means for causing the computer to represent the contact shapes as cells in a byte array; and

computer readable program code means for causing the computer to explore the conductor region shape by expanding into neighboring cells of the byte array.

19. (Previously Presented) The computer program product, according to claim 18, further comprising computer readable program code means for causing the computer to periodically skip expanding corner cells of the contact shapes.

20. (Previously Presented) The computer program product, according to claim 18, further comprising computer readable program code means for causing the computer to restrict the number of directions in which a cell in the byte array can expand.

21. (Currently amended) A method of performing latch up check on an integrated circuit (IC) design comprising the steps of:

computing a ~~combined least enclosing rectangle enclosing~~ rectangular shape that encloses a conductor region shape and contact shapes on the integrated circuit design, said rectangle shape being the smallest rectangular shape that completely encloses the conductor region shape and the contact shapes;

representing the contact shapes as cells in a byte array;

rasterizing the conductor region shape and the contact shapes;

iteratively expanding the contact shapes within the conductor region shape using a cellular algorithm;

generating shapes representing an unreachable area of the conductor region shape;

checking the shapes representing the unreachable area of the conductor region shape

against junction shapes in the design, and reporting to a designer any junction shapes which intersect the unreachable area as errors; and

extracting an unreachable area of the conductor region shape by traversing the byte array, row-by-row, detecting horizontal chains of unreachable cells, converting each chain into a rectangle by converting its corners into (X,Y) coordinate pairs representing positions in an original drawing space, and computing the union of these rectangles, and returning these shape(s) as the unreachable area of the conductor region.